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2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rosengaus et al.

Attorney Docket No.: KLA1P001C1

Application No.: 09/474,941

Examiner: Rosenberger, R.

Filed: December 30, 1999

Group: 2877

Title: SYSTEM AND METHOD FOR
INSPECTING SEMICONDUCTOR
WAFERS

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24.
R.C.E.
G. Stonly
8-29-01

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, or are being facsimile transmitted to the U.S. Patent and Trademark Office, on August 16, 2001.

Signed: _____

Lara M. Nelson

REQUEST FOR CONTINUED EXAMINATION (RCE)
UNDER 37 CFR §1.114

Commissioner for Patents
Box RCE
Washington, DC 20231

This is a Request for Continued Examination (RCE) of the above-identified application.

NOTE: If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. §1.53(d) instead of an RCE to be eligible for the patent term adjustment provisions of the AIPA.

1. Submission required under 37 C.F.R. §1.114:

- a. ☐ Previously submitted
- i. ☐ Consider the amendment/reply under 37 C.F.R. §1.116 previously filed on _____.
(Any unentered amendment referred to above will be entered.)
- ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____.
iii. ☐ Other _____.
- b. ☒ Enclosed
- i. ☒ Amendment/Reply
- ii. ☐ Affidavit/Declaration
- iii. ☐ Information Disclosure Statement with Form PTO-1449
☐ Copies of IDS Citations
- iv. ☐ Other _____.

08/21/2001 TBESHAH1 00000054 09474941

01 FC:179 710.00 OP
02 FC:103 180.00 OP
03 FC:102 240.00 OP
04 FC:125 110.00 OP
Created 06/00, Pat Prosec Transmittal RCE

2. **Fees:** (The RCE fee is required at the time the RCE is filed.)

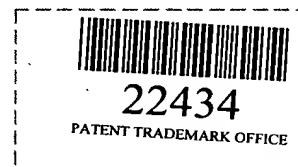
Fee Calculation (37 CFR §1.16)

	(Col. 1) Claims Remaining After Amendment		(Col. 2) Highest Number Previously Paid For	(Col. 3) Present Extra	Rate	Additional Fee
TOTAL	32	MINUS	22	= 10	x 18 =	180.00
INDEP.	07	MINUS	04	= 3	x 80 =	240.00
[] First presentation of multiple dependent claim					\$270 =	
Fee for Request for Continued Examination Under 37 C.F.R. §1.17(e)					\$710 =	710.00
TOTAL						710.00
SMALL ENTITY 50% FILING FEE REDUCTION (if applicable)						1,130.00

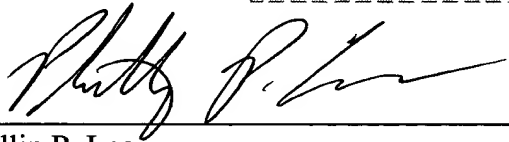
- ☒ a. Applicant hereby petitions for a 1month extension of time.
- ☒ b. Applicant believes that no (additional) extension of time is required; however, if it is determined that such an extension is required, Applicant hereby petitions that such an extension be granted and authorizes the Director to charge the required fees for an extension of time under 37 CFR §1.136 to Deposit Account No. 500388.
- ☒ c. Enclosed is our Check No. 12084 in the amount of \$1,240.00 to cover the RCE fee, any additional claim fee and/or extension of time fees.
- ☒ d. The Director is authorized to charge any fees beyond the amount enclosed which may be required, or to credit any overpayment, to Deposit Account No. 500388 (Order No. KLA1P001C1)

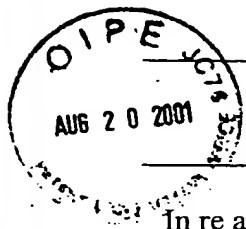
3. ☒ Please continue to send correspondence to the following address:

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Date: August 16, 2001


Phillip P. Lee
Registration No. 46,866



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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TECHNICAL CENTER 2000

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail to: Assistant Commissioner for Patents, Washington, DC 20231 on August 16, 2001.

Printed Name: Lara M. NelsonSigned: Lara M. NelsonAMENDMENT C

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The Examiner is respectfully requested to enter the following amendments and consider the following remarks.

IN THE CLAIMS:

Please AMEND claims 1, 6, 9 and 17 as follows:

1. An integrated circuit manufacturing system comprising:

(a) a plurality of interrelated integrated circuit manufacturing tools capable of operating in parallel on a plurality of semiconductor wafers, wherein the plurality of interrelated integrated circuit manufacturing tools comprise a cluster tool;

(b) a modular optical inspection system disposed proximate to a window of a cooling stage of the plurality of interrelated integrated circuit manufacturing tools, the modular optical inspection system being outside of a vacuum processing environment, the modular optical inspection system including